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MEMORY MODULE WITH HIERARCHICAL FUNCTIONALITY

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ABSTRACT OF THE DISCLOSURE

A hierarchical memory structure having memory cells, and sense amplifiers and decoders coupled with the memory cells to form first tier memory module, and subsequent tiers being formed by having *(n-1)*-tier memory modules, which are coupled with *(n)*-tier sense amplifiers and *(n)*-tier decoders. Also provided are a single-ended sense amplifier having sample-and-hold reference, and a charge-share limited-swing-driver sense amplifier; an asynchronously-resettable decoder; a wordline decoder having row redundancy; a redundancy device having redundant memory cells operated by a redundancy controller; a diffusion replica delay circuit; a high-precision delay measurement circuit; and a data transfer bus circuit imposing a limited voltage swing on a data bus. Methods are provided for a write-after-read operation without an interposed precharge cycle, and write-after-write operation with an interposed precharge cycle are provided, either operation being completed in less than one memory access cycle.

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